REMARKS

Applicants have reviewed the comments and rejections set forth by the Examiner in the Office Action dated January 21, 2005 and respectfully respond with the amendments above and the following remarks. Applicants respectfully thank the Examiner for accepting the formal drawings submitted in the above captioned matter on November 29, 2004.

Claims 8-9, 16, 20-27 and 29-30 are pending in the present case. Claims 8-9, 16, 20-27 and 29-30 are amended herein. Claims 6-7, 14-15, 17-19 and 28 are cancelled herein. No new matter is added. Applicants respectfully request reconsideration in view of the above amendments and the arguments set forth below.

CLAIM REJECTIONS

Claims 6-9, 25 and 26, Claims 14-16 and 23-24, Claims 18-20 and 21-22, and Claims 27-30 are rejected under 35 USC 102(e) over US Patent No. 6,762,466 B2 to Huang, et al. (hereinafter Huang). Claims 6-7, 14-15, 17-19 and 28 are cancelled herein. Thus, Applicants respectfully assert that their rejection is moot. Further, Applicants have reviewed the reference cited and respectfully assert it does not teach or suggest the embodiments of the present invention as recited in Claims 8-9, and 25-26, Claims 16 and 23-24, Claims 20-22, Claim 27 and 29-30 for the following rationale.

As Applicants understand the reference, Huang teaches "a circuit structure for connecting the bonding pad of a semiconductor device with an electrostatic discharge (ESD) protection circuit ..." and to do so such "that line width of the conductive connection wire can be reduced, thereby increasing the manufacturing process

window." Huang, col. 2, ll. 15-24. Huang expressly teaches that the multiple current carrying pathways therein allow smaller "line widths" allow "more flexibility in circuit design," (Id. at ll. 52-54) and to allow continuing ESD protection even "when one of these [conductors] is accidentally severed." (Id. at ll. 56-59). The teaching of Huang thus differs from the embodiments of the present invention recited in Claims 8-9 and 25-26.

Claims 9, 25 and 26 depend on independent Claim 8. As amended herein, Claim 8 reads as follows, with underlining added for emphasis:

> 8. A semiconductor structure comprising:
> a pad area;
> an electrostatic discharge protective device disposed directly below said pad area, said electrostatic discharge protective device comprising a transistor and a resistance, wherein said pad area comprises:
> a substrate;
> a first layer of metal disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal; and
> a second layer of metal disposed above said first layer of metal;
> a layer of dielectric disposed between said first metal layer and said second metal layer; and
> a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias, wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another and wherein a resistive value of said resistance is configurable during a process for fabricating said semiconductor structure, wherein said resistive value of said resistance is fixed therein with setting a particular number for said portion of said plurality of individual vias in parallel.

Independent Claims 16, 20 and 27 are amended herein after a similar fashion.

Claims 23-24, Claims 20-22, and Claim 29-30 respectively depend on Claims 16, 20 and 27.

Claims 8, 16, 20 and 27, as amended herein, recite that a semiconductor structure has an electrostatic discharge protective device (hereinafter ESPD) disposed directly below a pad area thereof. The semiconductor structure also has a via, comprising a plurality of individual vias arranged in parallel, which comprise a portion of the resistance of the ESPD. The resistive value corresponding to the ESDP resistance is configurable during fabrication of the semiconductor structure, with setting a particular number of the individual vias in parallel.

Forming a semiconductor structure with an ESDP, including its resistive components, such as a resistance, directly below its pad area, as recited in Claims 8, 16, 20 and 27, has advantages related to efficient use of the available semiconductor material, device and circuit layout, and concomitant economic savings. Further, as described in the original specification from lines 29-39 at page 12 and from lines 9-11 at page 15, embodiments of the present invention recited in Claims 8, 16, 20 and 27 allow the resistive value of the ESPD resistance to be readily configured during fabrication of the semiconductor structure, with setting a particular number of the individual vias, as a component of the ESDP resistance has advantages relating to economics and efficiency of fabrication.

Moreover, besides configuring the ESDP resistance with setting a particular number for the portion of the plurality of individual vias in parallel, embodiments recited herein also allow the ESDP resistance to be configured with forming individual vias comprising the portion of the plurality of individual vias with a particular cross

sectional area and/or forming the individual vias comprising the portion of the plurality of individual vias with a particular length.

Applicants have reviewed the Huang reference and find no teaching therein directed towards a semiconductor structure that has an ESDP device disposed directly below the pad area thereof, as recited in Claims 8, 16, 20 and 27 herein. In fact, with reference to Figure 3 therein, Huang's ESDP transistor 218 is clearly depicted as displaced horizontally from positioning directly under Huang's pad area 200. Thus, Applicants respectfully assert that the Huang reference does not teach or suggest the embodiments recited in Claims 8, 16, 20 and 27 and their respective dependent claims, and in fact, that the reference expressly teaches away therefrom.

Further, while Applicants agree with the Examiner's observation relating to Huang that "the fabrication determines the amount of polysilicon used, and therefore fixes the overall resistance," (present OA at 2-5), Applicants respectfully assert that Huang's express teaching in this area differs from the embodiments recited in Claims 8, 16, 20 and 27 herein. These recited embodiments allow the resistance associated with the ESDP to be configurable during fabrication. Applicants find no such teaching in Huang.

In fact, in Huang's express teachings that (1) the multiple current carrying pathways therein allow smaller "line widths," which allow "more flexibility in circuit design" (Op. Cit. at ll. 52-54), and (2) allow continuing ESD protection even "when one of these [conductors] is accidentally severed" (Op Cit. at ll. 56-59) both implicitly teach away from the embodiments recited in Claim 8, 16, 20 and 27, wherein the

ESDP resistance is configurable. For instance, Huang's "flexibility in circuit design" (Op. Cit.) implies improved versatility in conductor layout therein, as opposed to configurability of the ESDP's associated resistance. This implication is reinforced by Huang's express statement that the ESDP taught therein remains functional after accidental severing of one of the conductors (Op. Cit.), which implies that, rather than configuring a resistance value from paralleled vias, as recited herein, Huang's ESDP resistance does not depend upon a particularly configured resistance and/or upon a particularly configured number of vias.

Applicants do not any teaching or suggestion in Huang to dispose an ESDP device directly under a pad, nor to configure ESDP resistance values with fixing a particular number of parallel vias in fabrication. Applicants also respectfully assert that the reference expressly and implicitly teaches away from the embodiments recited herein. Thus, Applicants respectfully assert that Huang does not teach or suggest the embodiments recited in Claims 8, 16, 20 and 27 and their respective dependent claims.

CONCLUSION

By the rationale stated above, Applicants respectfully assert that Claims 8, 16, 20 and 27 and their respective dependent claims are allowable over the cited reference under 35 USC 102(e). Applicants respectfully assert therefore that Claims 8-9, 16, 20-27 and 29-30 are in condition for allowance.

Accordingly, Applicants respectfully request that the rejection of Claims 8-9, 16, 20-27 and 29-30 under 35 U.S.C. 102(e) be withdrawn and that Claims 8-9, 16, 20-27 and 29-30 be allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

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Dated: April 20, 2005

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